REMARKS

This paper is responsive to the Office Action mailed from the Patent and Trademark Office on June 16, 2004, which has a shortened statutory period set to expire September 16, 2004.

Drawings

The drawings are objected to on page 3 of the Office Action as failing to comply with 37 CFR 1.84 (p)(5) for failing to include the reference numeral "300".

In the appended "redline" sheet, Fig. 3 is amended to include reference numeral "300", thus addressing the pending objection. The "redline" sheet and corresponding replacement sheet including the above-mentioned amended Fig. 3 is entered under the Submission of Proposed Drawing Amendment, which is submitted with this paper.

No new matter is introduced by the amendment to Fig. 3. Reconsideration and withdrawal of these objections is therefore respectfully requested.

Specification

Paragraphs 0007, 0010 and 0027-0029 of the specification are amended according to the helpful comments raised in paragraph 3 of the Office Action.

No new matter is introduced by any of the amendments to the specification. Reconsideration and withdrawal of these objections is therefore respectfully requested.

Claims

Claims 1-20 are pending in the above-identified application. Claim 1 is rejected under 35 USC 112, and Claims 1-4, 7, 15 and 19 are rejected under 35 USC 103for reasons set forth below. Claims 5, 6, 8-14, 16-18 and 20 are objected to as being dependent from a rejected base claim, but are otherwise indicated as being allowable.

In the current paper, Claims 1, 5, 6 and 18 are amended, and Claims 2-4, 7-17, 19 and 20 remain as filed. No new matter is entered. Reconsideration and withdrawal of the pending rejections in view of the following remarks is respectfully requested.

Claim Objections

Claim 18 is amended in response to the objection raised in paragraph 4 (page 3) of the Office Action. No new matter is entered, and Applicants respectfully request reconsideration and withdrawal of the pending objections to Claim 18.

Rejection Under 35 USC 112

Claim 1 is rejected under 35 USC 112 for reciting "first memory". Claim 1 is amended to recite "first array" per the Examiner's helpful comment. No new matter is entered by the above-listed amendments, and Applicants respectfully request reconsideration and withdrawal of the pending rejection to Claim 1.

Rejection Under 35 USC 103

Claims 1-4, 7, 15 and 19 are rejected under 35 USC 103(a) as being unpatentable over Jang et al. (USP 6,640,354; herein "Jang") in view of Ledford et al. (USP 6,347,056; herein "Ledford").

Claim 1 is amended to clarify that the control circuit includes "means for sequentially reading the self-test instructions from the first array during a first operating phase, a command register for receiving the self-test instructions sequentially read from the first array during the first operating phase, and for executing the self-test instructions during a second operating phase, whereby the data values are read from the second array in response to execution of at least one of said self-test instructions, and a comparator circuit for detecting defective non-volatile memory cells in the second array by comparing the data values read in response to said at least one self-test instruction with predefined values during the second operating phase." Support for this amendment is found, for example, in paragraph 0009 of Applicants' specification (page 4):

> In accordance with the present invention, a non-volatile memory device is provided in which self-test instructions are loaded from a tester into a special (configuration) array of memory cells, and a special control circuit of the memory device then sequentially reads and executes the self-test instructions while the tester is in an idle state (i.e., transmitting neither data nor address signals to the memory device). During the execution of the self-test instructions, data patterns are written to and read from the main memory array according to the stored self-test instructions.

In rejecting Claim 1, the Examiner writes (in pertinent part):

> ...Jang does not explicitly teach that the self-test instructions are stored in a first array...Ledford suggests algorithmic parameters are stored in non-user addressable locations (first array) Electrically Erasable Array 46 (non-volatile memory cells)...It would have been obvious to one of ordinary skill in the art at the time the invention was made [sic, to

> combine] Jang's DRAM memory cell array 62 with Ledford's Electrically Erasable Array 46 for storing the test parameters (self-test instructions) and data patterns. The artisan would have been motivated to do so because this would because it would enable Jang to store self-test instructions in memory that would be retained if power was lost. Also, it would lend Jang the flexibility to modify the self-test instructions in the Electrically Erasable Array 46.

As amended, Claim 1 is believed to be distinguished over Jang and Ledford at least because neither of these references teach or suggest "means for sequentially reading the self-test instructions from the first array during a first operating phase" and "a command register for receiving the self-test instructions sequentially read from the first array during the first operating phase, and for executing the self-test instructions during a second operating phase, whereby the data values are read from the second array in response to execution of at least one of said self-test instructions" as recited in Claim 1.

Moreover, it would not have been possible to combine the teachings of Jang and Ledford to produce the non-volatile memory device recited in amended Claim 1. As set forth in the above-quoted rejection, the Examiner admits "Jang does not explicitly teach that the self-test instructions are stored in a first array". Similarly, although the Examiner appears to correctly point out that Ledford teaches storing "parameters" in Electrically Erasable Array 46, these "parameters" are simply not "self-test instructions" that are subsequently executed by a "command register" such that "data values are read from the second array in response to execution of at least one of said self-test instructions" as recited in Claim 1. Instead, Ledford appears to teach at Col. 4, lines 45-48 that the test algorithms

utilized by Ledford's circuit are executed by state machines, such as State Machine 70:

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> The programming of the data is under control of a test algorithm being executed by State Machine **70**. State Machine **51** launches State Machine **70** with a single command to begin execution of a predetermined test algorithm.

Ledford then teaches at Col. 5, lines 18-25 that the "parameters" read from Electrically Erasable Array 46 are "required by" the test algorithms executed by to State Machine 70 (i.e., values utilized by the executed algorithm, as distinguished from the executed algorithm instructions):

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> Subsequent to the initialization mode, Electrically Erasable Array **46** may provide to Timer **72** and other portions of Memory Interface **34** stored parameters (e.g. timing, algorithm modifiers, etc.) required by algorithms used by the State Machine **70** to program, erase, read and stress test Electrically Erasable Array **46**. Such stored parameters are stored in Electrically Erasable Array **46** typically in non-user addressable locations.

Accordingly, it would have been neither possible nor obvious to combine the teachings of Jang and Ledford to produce the non-volatile memory device of Claim 1 because neither of these references teach or suggest "means for sequentially reading the self-test instructions from the first array during a first operating phase" and "a command register for receiving the self-test instructions sequentially read from the first array during the first operating phase, and for executing the self-test instructions during a second operating phase", as recited in Claim 1.

Claims 2-4 are dependent from Claim 1, and are believed to be distinguished over Jang and Ledford for at least the reasons provided above with reference to Claim 1.

Similar to Claim 1, Claim 7 recites a method for performing wafer sort testing on a non-volatile memory device including (in part) "storing a series of self-test instructions transmitted from the tester in the first array of the non-volatile memory device...reading the first instruction from the first array and transferring the first instruction to a command register of the control circuit, wherein the first instruction includes a pre-determined data pattern; and writing the predetermined data pattern to a second array of non-volatile memory cells in accordance with the first instruction stored in the command register." Accordingly, Claim 7 is believed to be distinguished over Jang and Ledford for reasons similar to those provided above with reference to Claim 1.

Similar to Claims 1 and 7, Claim 15 recites a method for performing wafer sort testing on a non-volatile memory device including (in part) "storing a self-test instruction transmitted from the tester in the first array of the non-volatile memory device; reading the self-test instruction from the first array and transferring the self-test instruction to a command register of the control circuit, wherein the self-test instruction includes a predetermined data pattern; reading data values from the second array of non-volatile memory cells in accordance with the self-test instruction..." Accordingly, Claim 15 is believed to be distinguished over Jang and Ledford for reasons similar to those provided above with reference to Claim 1.

Finally, similar to Claims 1, 7 and 15, Claim 19 recites a method for performing wafer sort testing on a non-volatile memory array including (in part) "writing a series of self-test instructions into first memory cells of the non-volatile memory array; transmitting a start command that causes the non-volatile memory array to sequentially read the series of self-test instructions from the first memory cells, and to execute the self-test instructions..." Accordingly, Claim 19 is believed to be distinguished over Jang and Ledford for reasons similar to those provided above with reference to Claim 1.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of the rejections under 35 USC 103.

Allowable Subject Matter

Claims 5, 6, 8-14, 16-18 and 20 are objected to as being dependent on a rejected base claim, but are otherwise indicated as being allowable.

Claim 5 is amended to incorporate the subject matter of Claim 1 (as filed), and is therefore believed to be in condition for allowance.

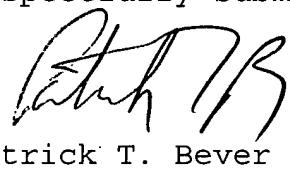
Claim 6 is dependent from Claim 5, and is therefore also believed to be in condition for allowance.

Claims 8-14, 16-18 and 20 are believed to be allowable at least for the reasons provided above with reference to Claims 7, 15, and 19, respectively.

CONCLUSION

Claims 1-20 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested. If there are any questions, please telephone the undersigned at (408) 451-5902 to expedite prosecution of this case.

Respectfully submitted,



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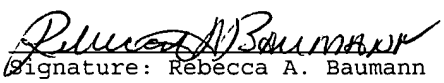
Signature: Rebecca A. Baumann

REDLINE

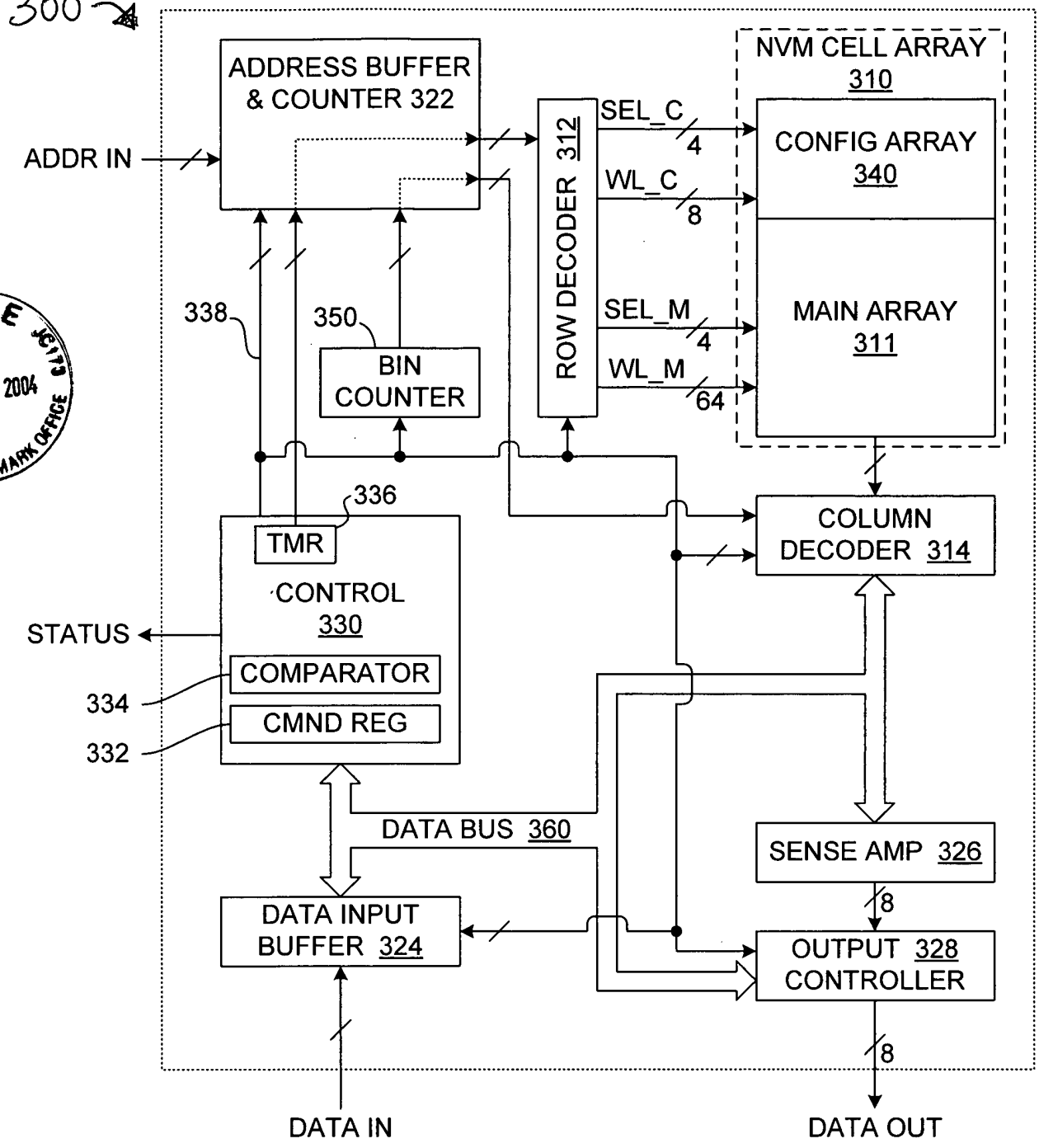

FIG. 3